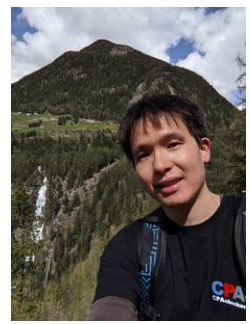
Bridging Hardware and Software Formal Verification for Reliable Computing Systems

Nian-Ze Lee

LMU Munich, Germany

April 7, COOP 2024



LMU LUDWIG-MAXIMILIANS-UNIVERSITÄT MÜNCHEN

SoSy-Lab Software Systems

About Me

- Since 2021, PostDoc in Computer Science, LMU Munich
- 2021, Ph.D. in Electronics Engineering, NTU, Taipei

Modern Computing Systems

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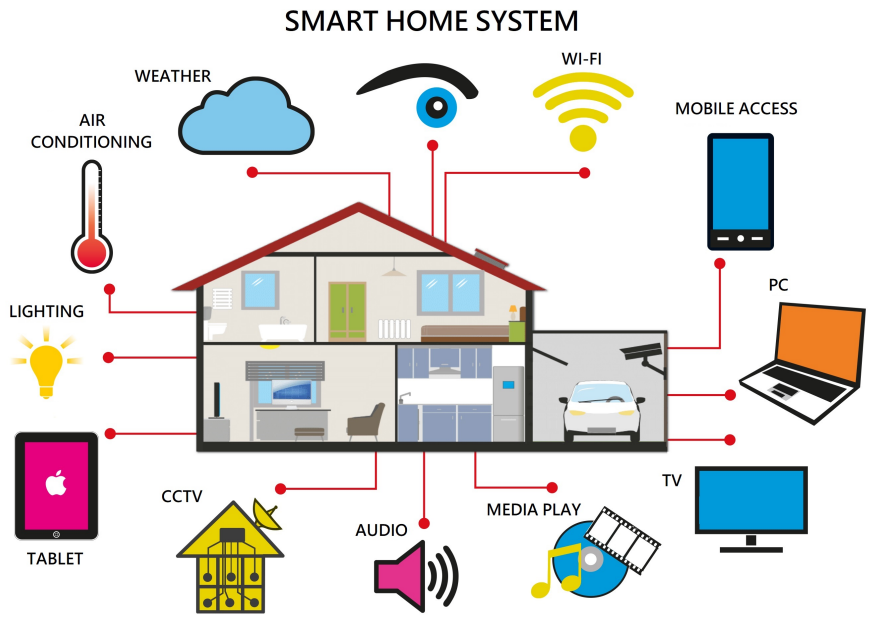

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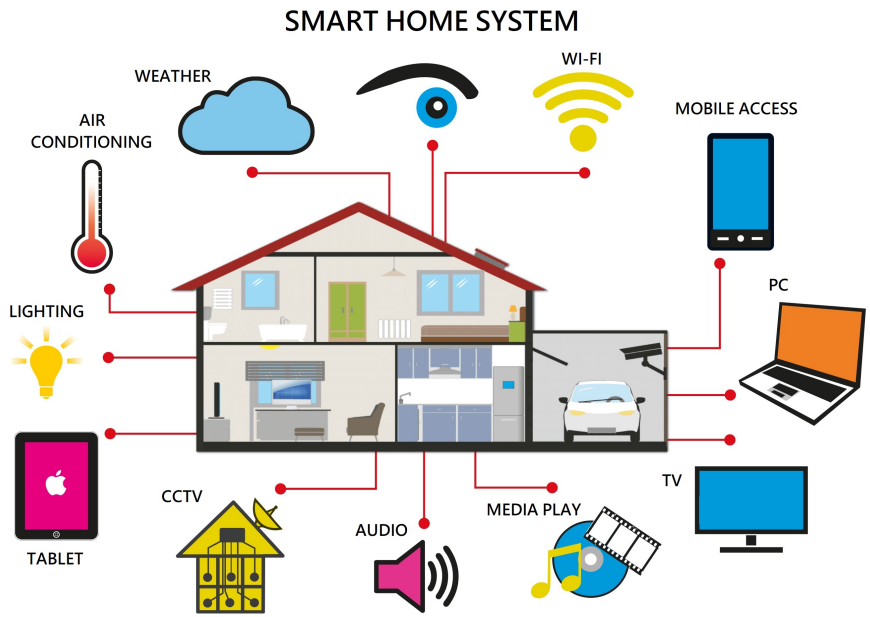

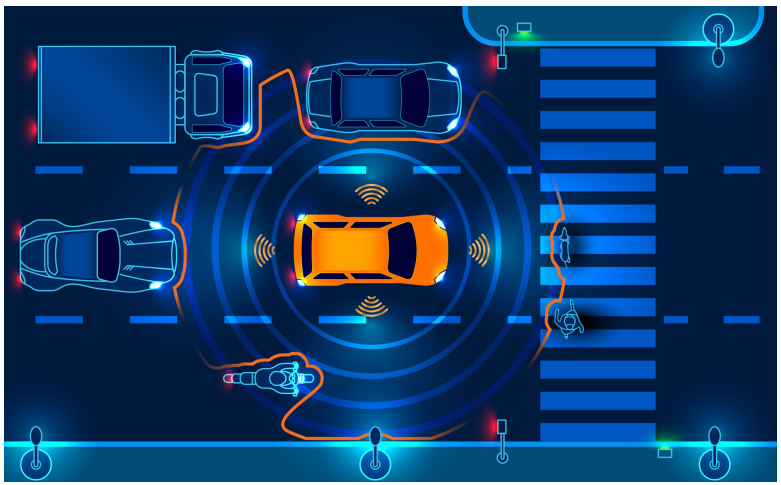

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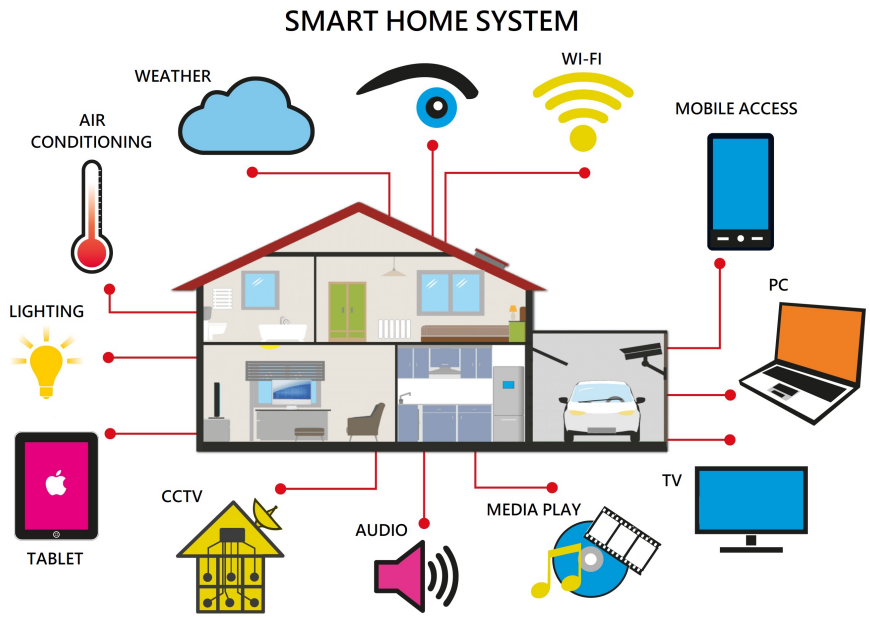

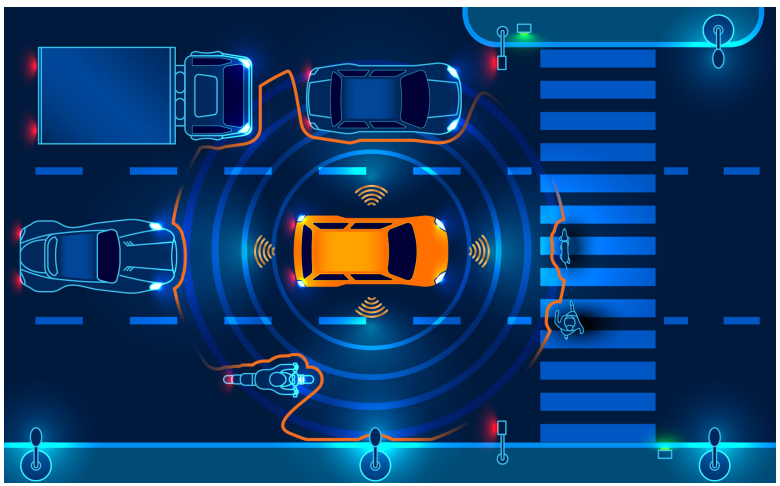

*Images from the Internet

Heterogeneous Components

- Hardware VLSI circuits
- Software programs
- Cyber-physical devices

Challenges of Analyzing Heterogeneous Systems

- Complex interactions
- Distributed computing
- Modeling difficulties

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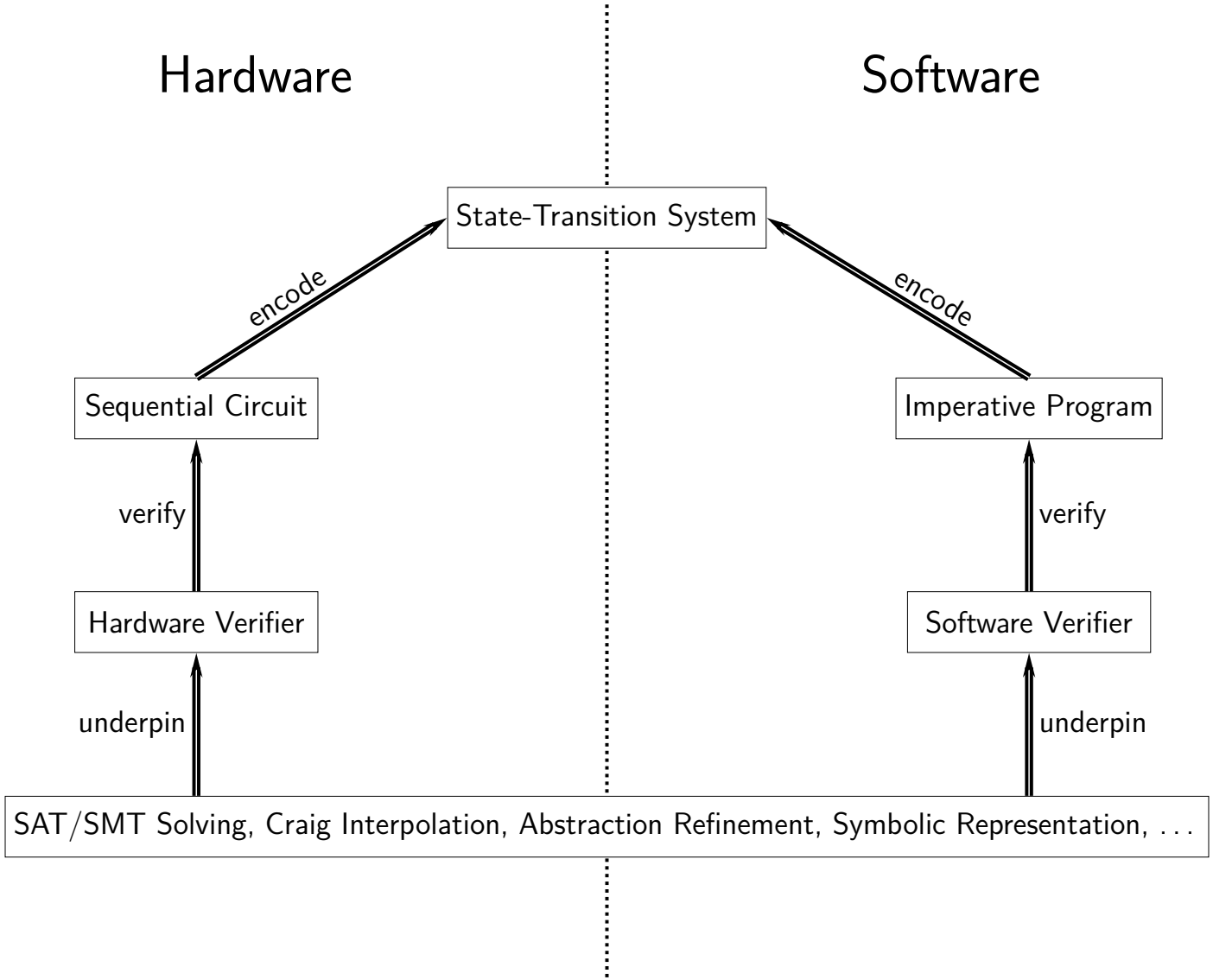
Cooperative and cross-disciplinary approaches are necessary. We should know the state of the art before developing new methods to avoid reinventing the wheel!

Conventional HW and SW Formal Verification



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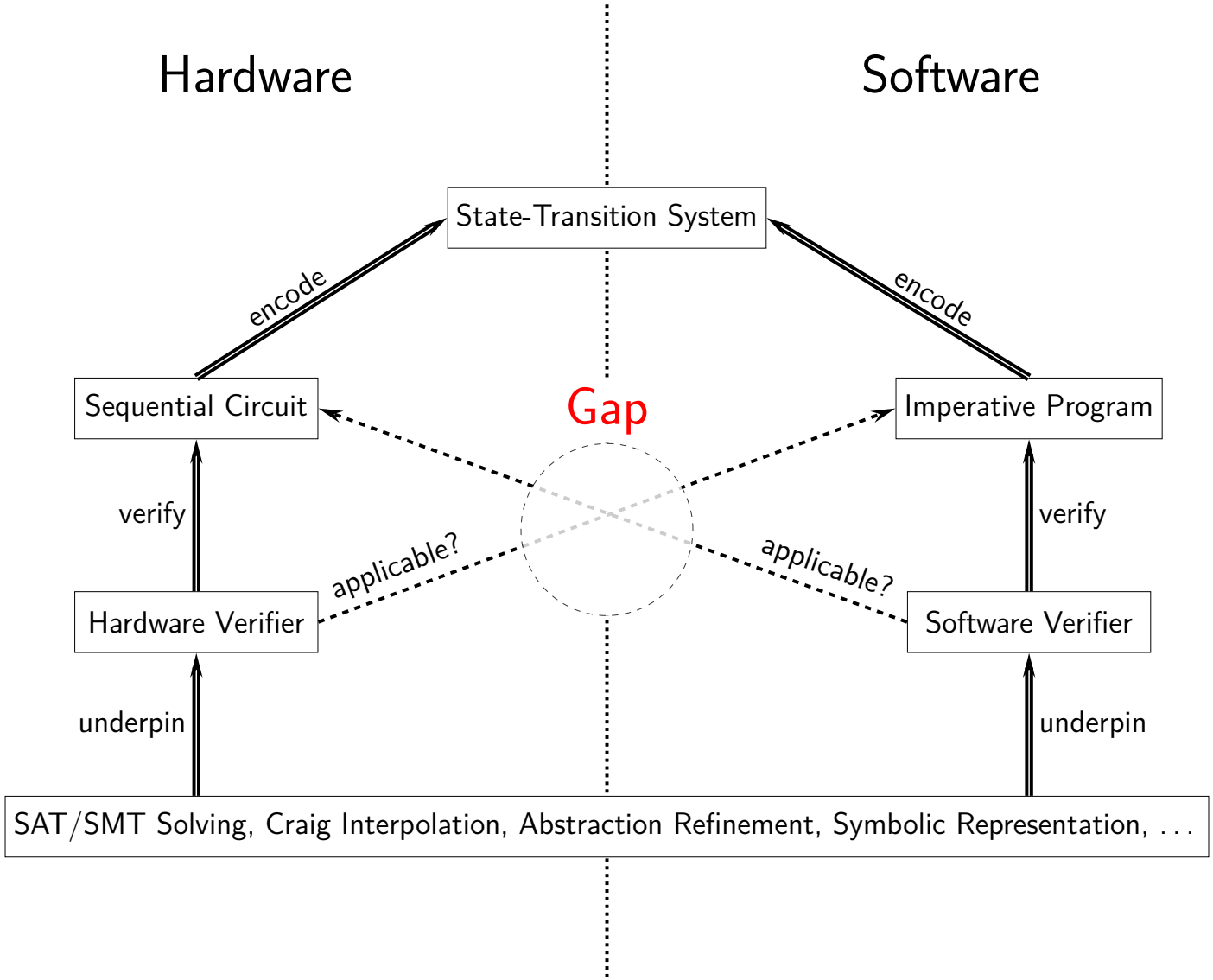

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- Current work
  - Cross-application of each other's advancements
  - Consolidation of formal-verification knowledge

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Hardware-verification algorithms can improve software verifiers.

- Outlook: collaboration/mutual learning for new challenges
  - Scalable full-stack verification of the entire system
  - Neural networks, embedded or cyber-physical systems

Agenda

1. Cross-application of HW and SW formal verification
1.1 Applying SW analyzers to HW verification tasks
1.2 Applying HW model checkers to SW verification tasks

2. Knowledge consolidation of formal verification
2.1 Transferability of HW algorithms to SW verification

3. Reflection and outlook

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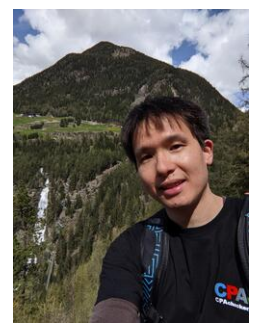
Bridging Hardware and Software Analysis with Btor2C: A Word-Level-Circuit-to-C Translator

Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee

LMU Munich, Germany

Published at the 29th International Conference on

Tools and Algorithms for the Construction and Analysis of Systems (TACAS), 2023



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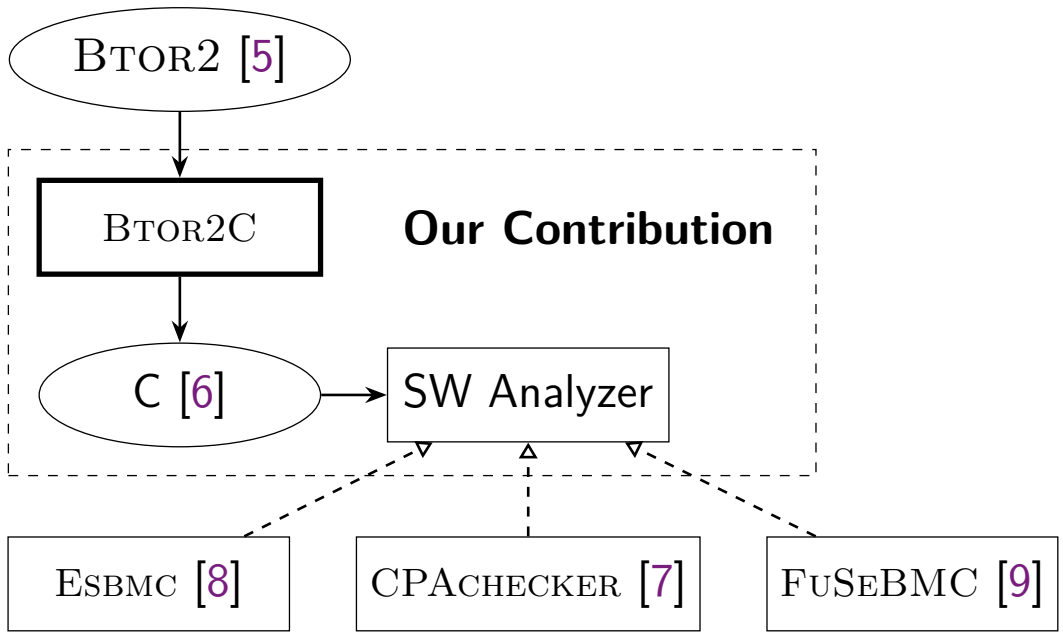
43 HW-verification tasks uniquely solved by SW analyzers in our evaluation $\rightarrow$ enhance HW quality assurance

Our Contribution



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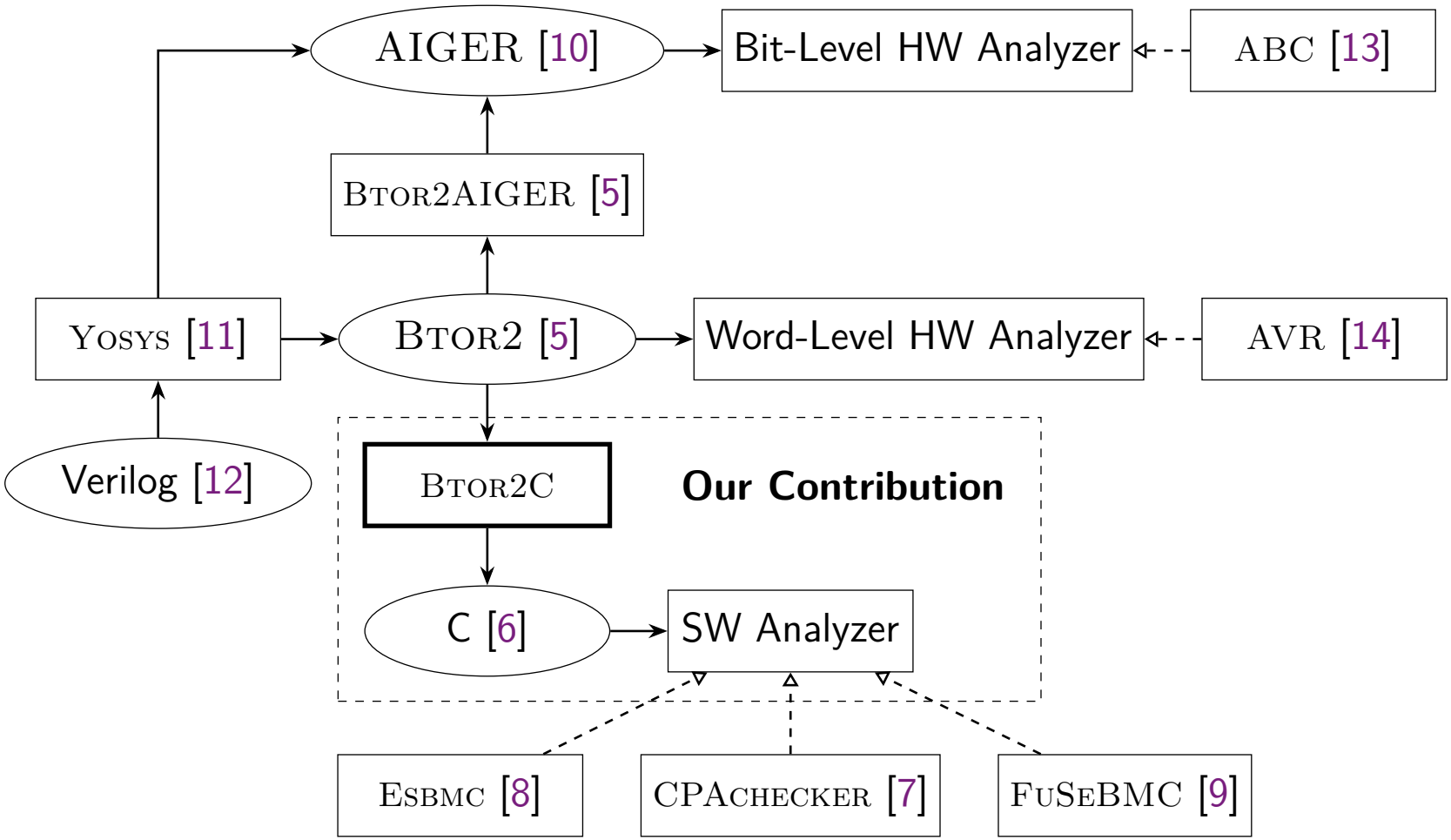

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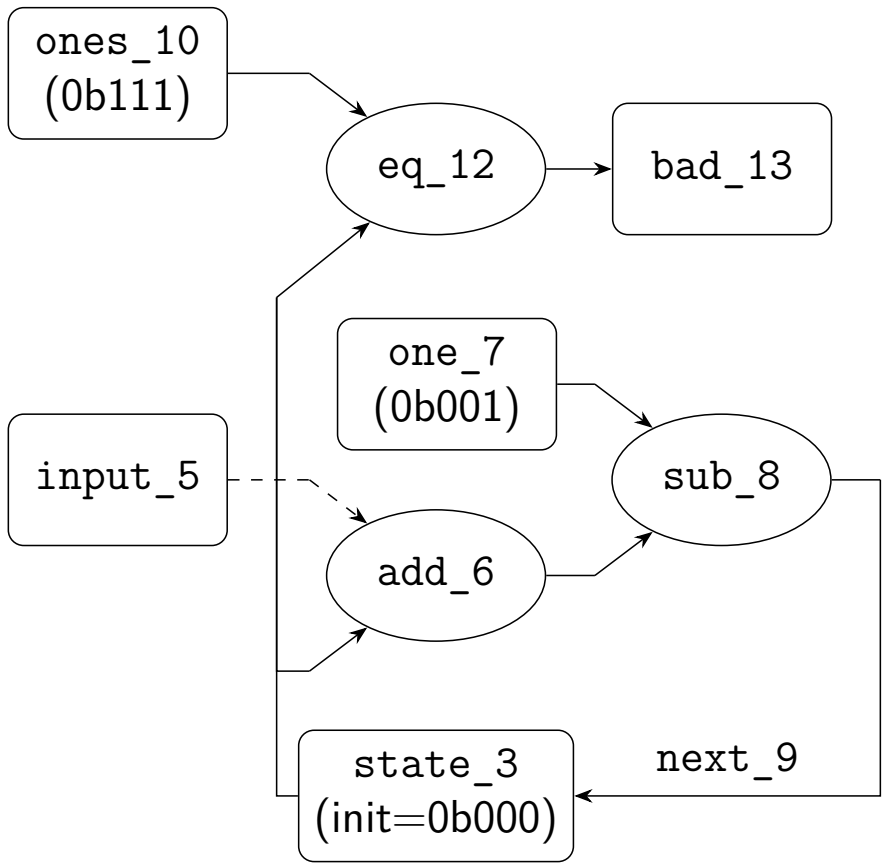

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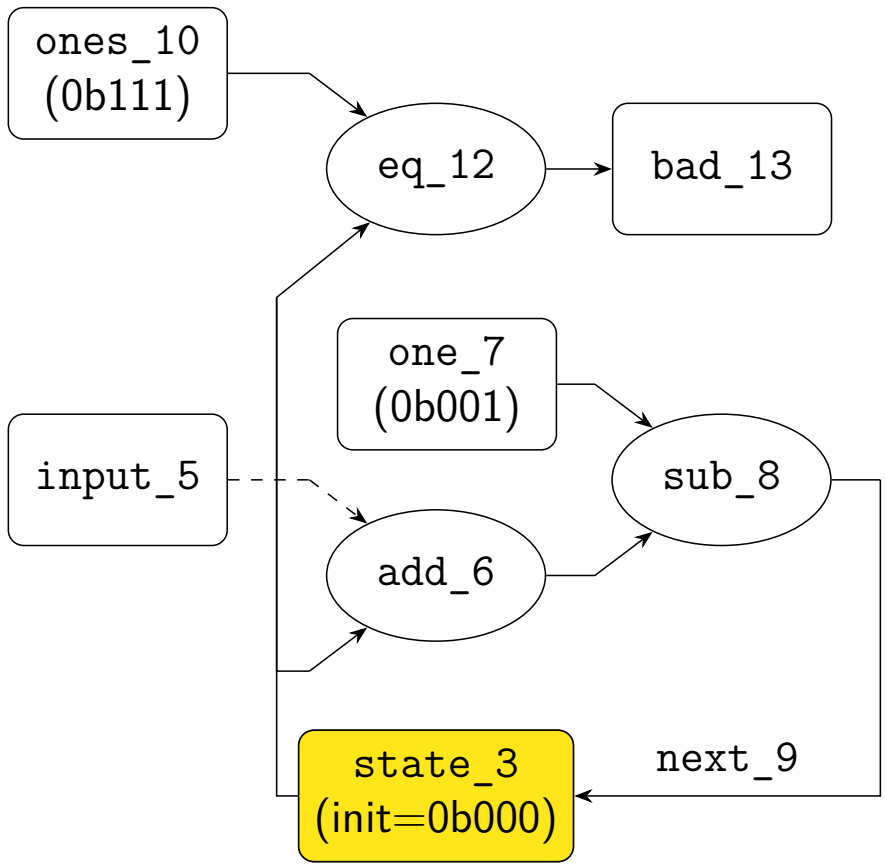

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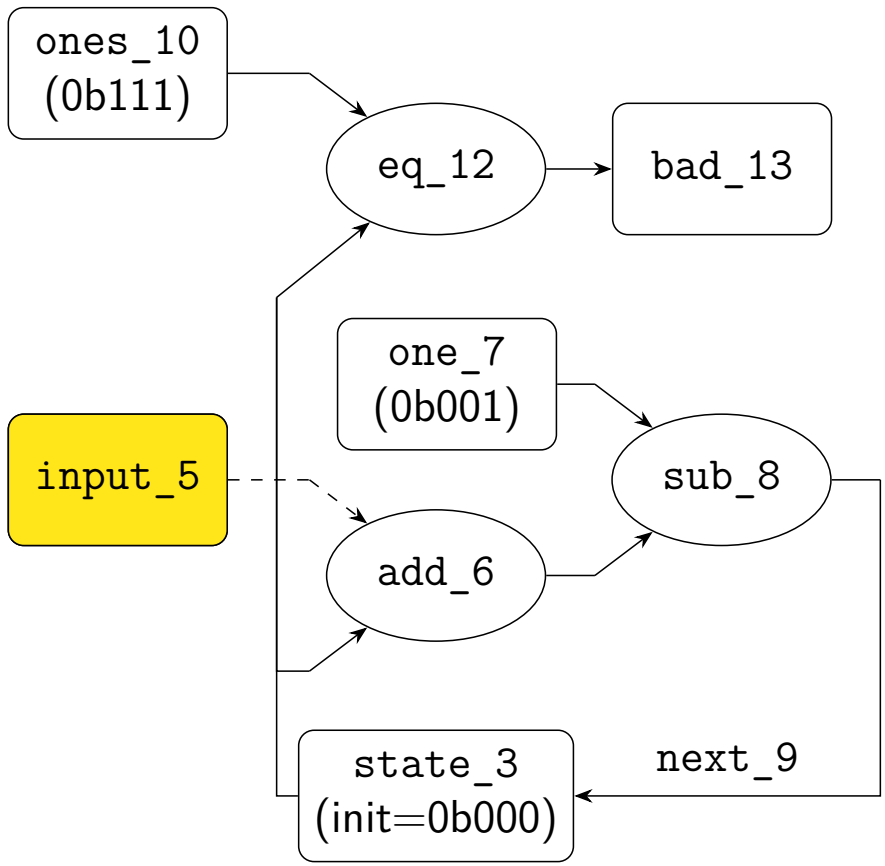

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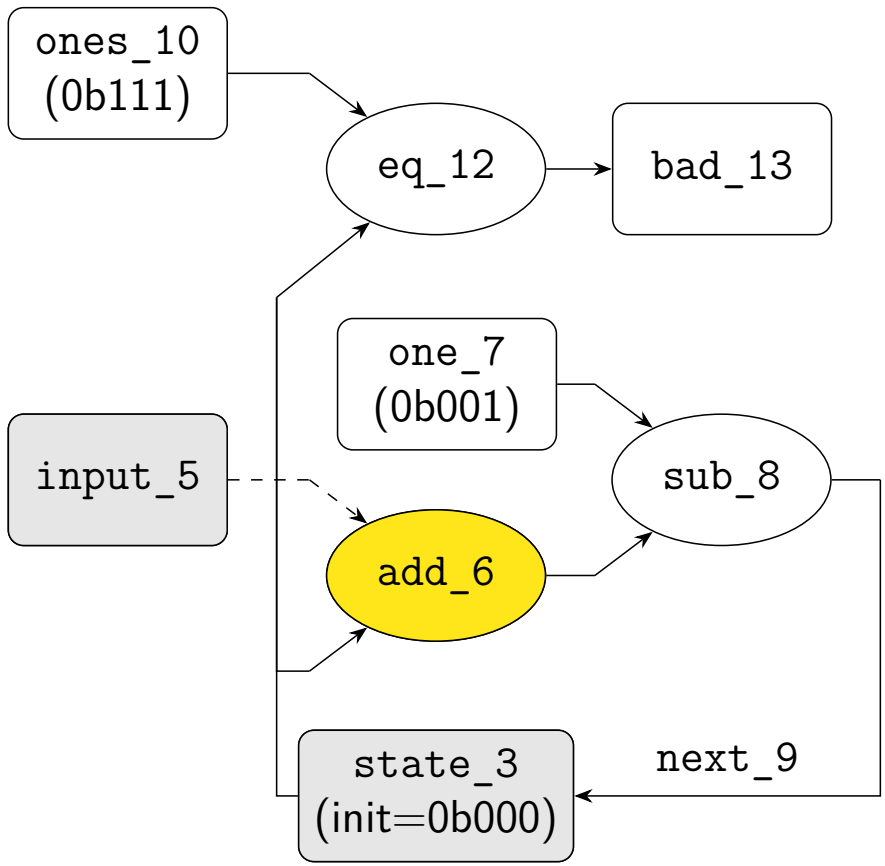

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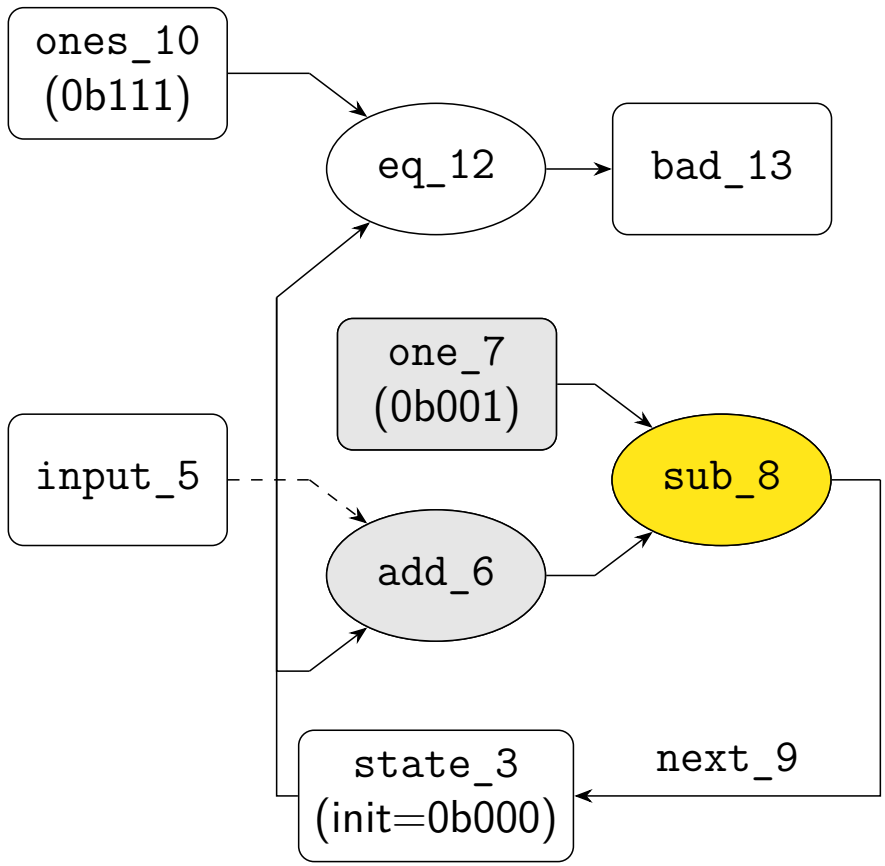

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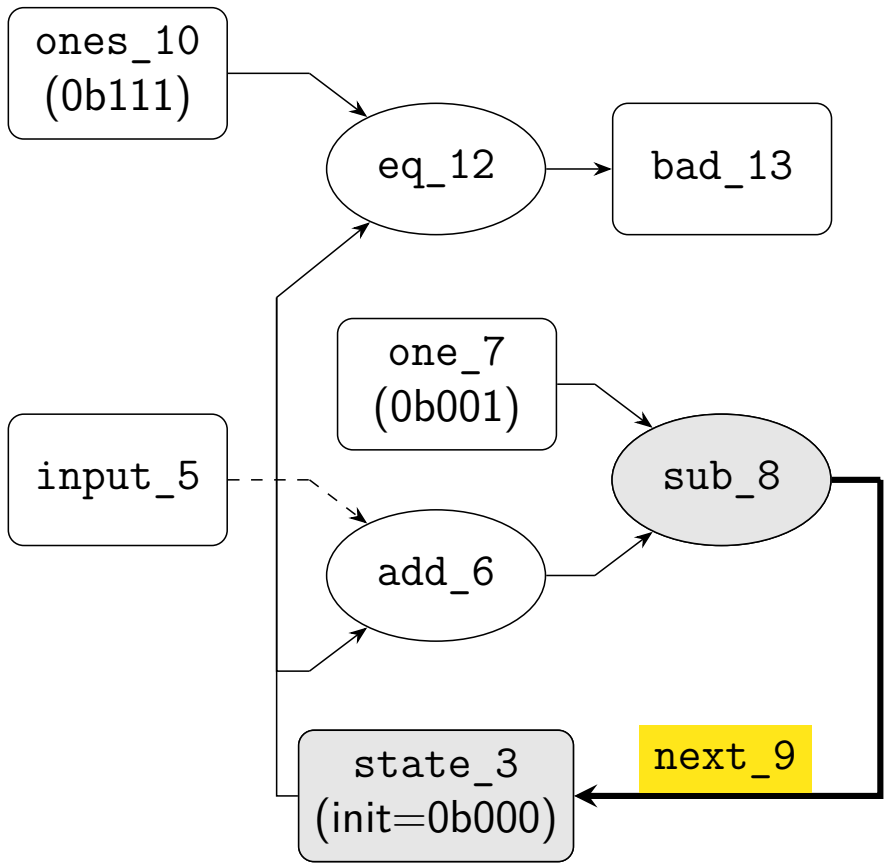

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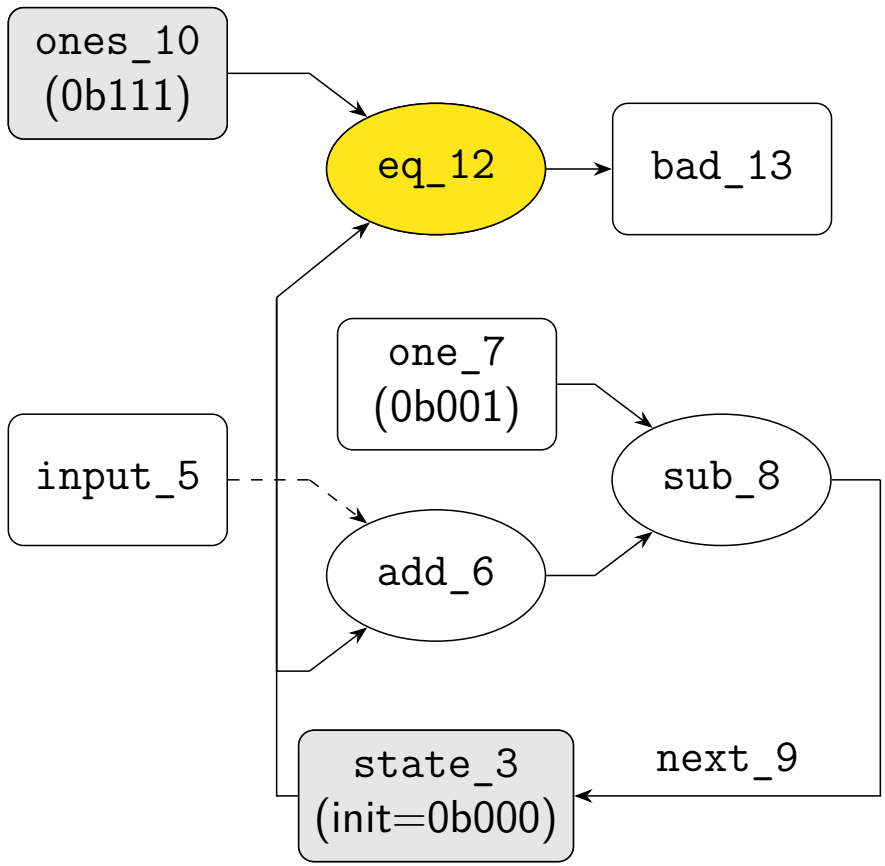

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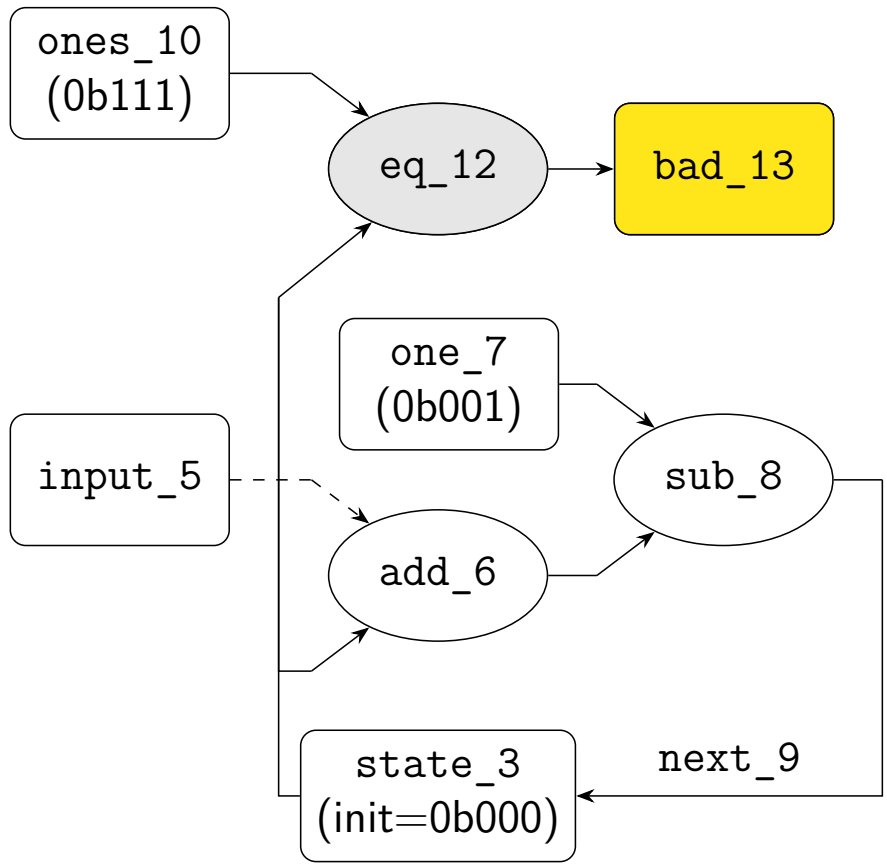

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Btor2C: Btor2-to-C Translator

- A lightweight tool
  - Written in C++ with $\sim$2 K LOC
  - Use the frontend parser provided by Btor2Tools [17]
- Open-source under Apache License 2.0:
  https://gitlab.com/sosy-lab/software/btor2c

Evaluation

On $1\,008$ safe and 490 unsafe BTOR2 verification tasks:

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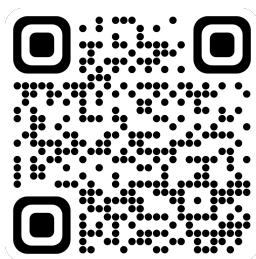
On $1\,008$ safe and 490 unsafe BTOR2 verification tasks:

- **RQ1**: How do SW analyzers perform on HW tasks?
  Quite decent! Each analyzer showcases different strength
- **RQ2**: Can SW analyzers complement HW model checkers?
  *Yes, **43** tasks were uniquely solved by SW verifiers*

Summary

- Btor2C: Btor2 circuits to C programs
  - Applying off-the-shelf software analyzers to hardware
  - Improving quality assurance for hardware
- **43** tasks uniquely solved by software verifiers
- The reproduction artifact [23] is available via Zenodo.



Btor2-Cert: A Certifying Hardware-Verification Framework Using Software Analyzers

Zsófia Ádám[1,2], Dirk Beyer[2], Po-Chun Chien[2],
Nian-Ze Lee[2], and Nils Sirrenberg[2]

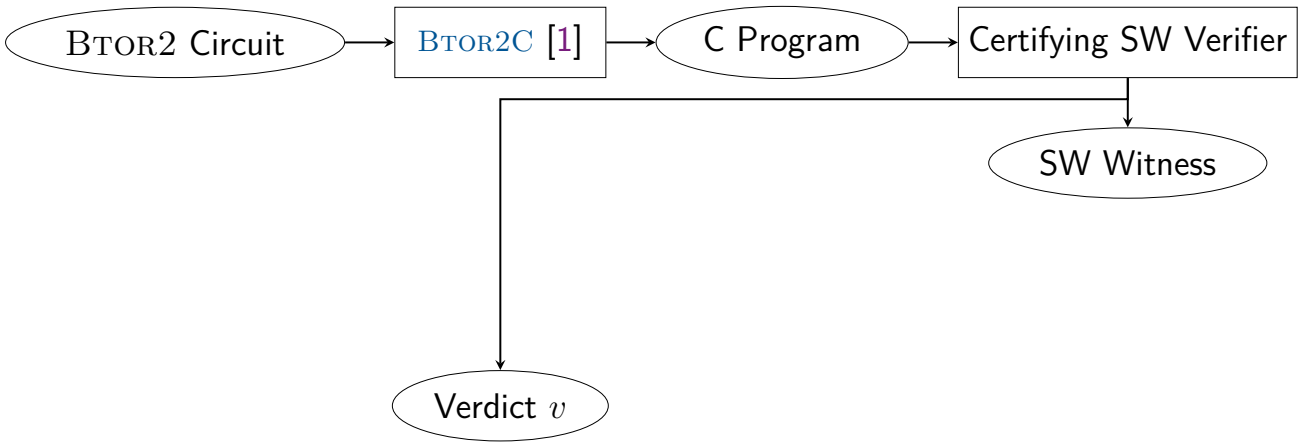
[1]Budapest University of Technology and Economics, Hungary
[2]LMU Munich, Germany

TACAS 2024-04-11





Certifying Verification for BTOR2 with SV Tools



- BTOR2 [5] word-level circuits and translator BTOR2C [1]
- Software verifiers in SV-COMP [24]

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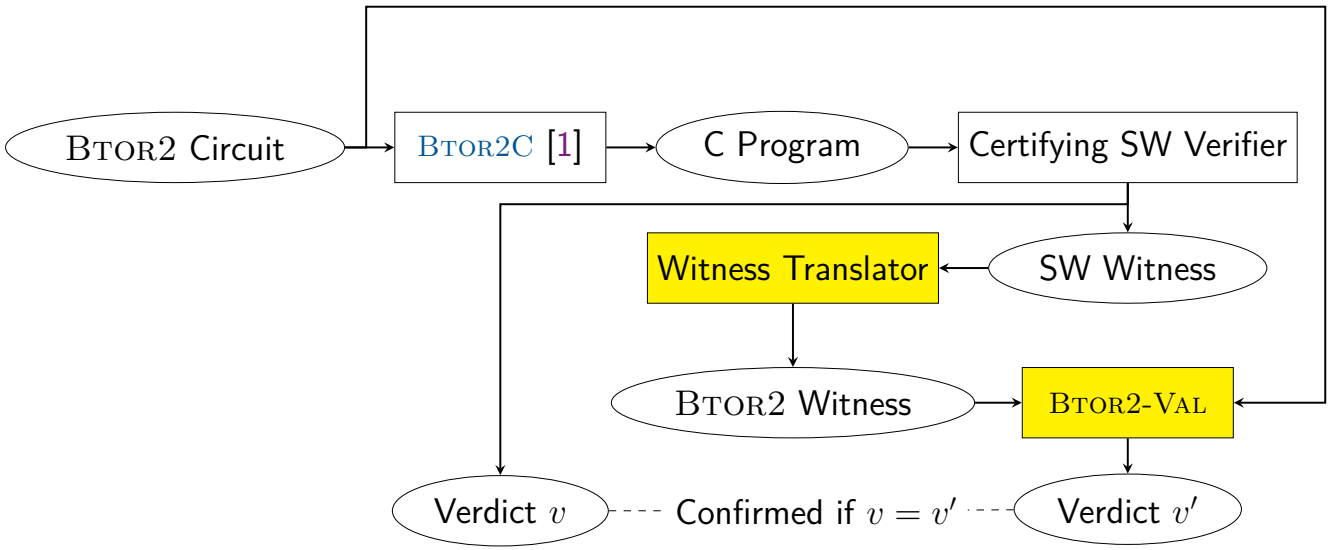

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- SW-to-HW witness translation and BTOR2-VAL

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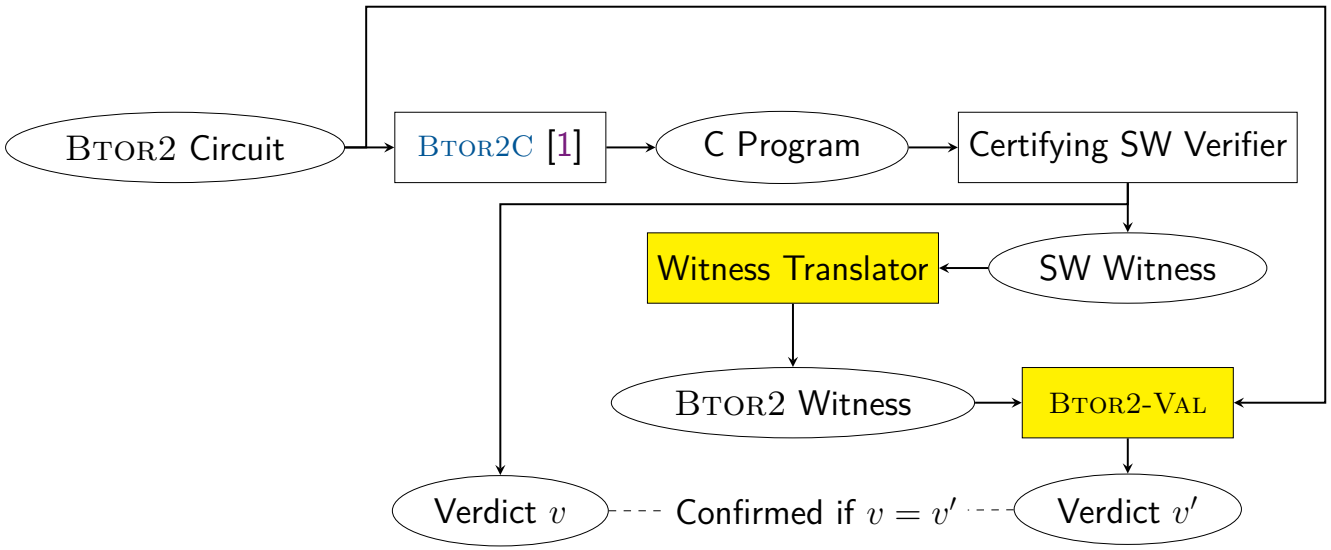

- BTOR2 [5] word-level circuits and translator BTOR2C [1]
- Software verifiers in SV-COMP [24]
- SW-to-HW witness translation and BTOR2-VAL
- On 1214 BTOR2 circuits, BTOR2-CERT
  - found missed bugs by CBMC [25] to complement ABC [13]
  - derived invariants by CPACHECKER [7] to accelerate ABC

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CPV: A Circuit-Based Program Verifier

Po-Chun Chien and Nian-Ze Lee

LMU Munich, Germany

First-Time Participant at SV-COMP 2024 (April 8)

Research Question

- Sequential circuits as an alternative intermediate representation for program analysis
  - Leveraging HW model checking as backend

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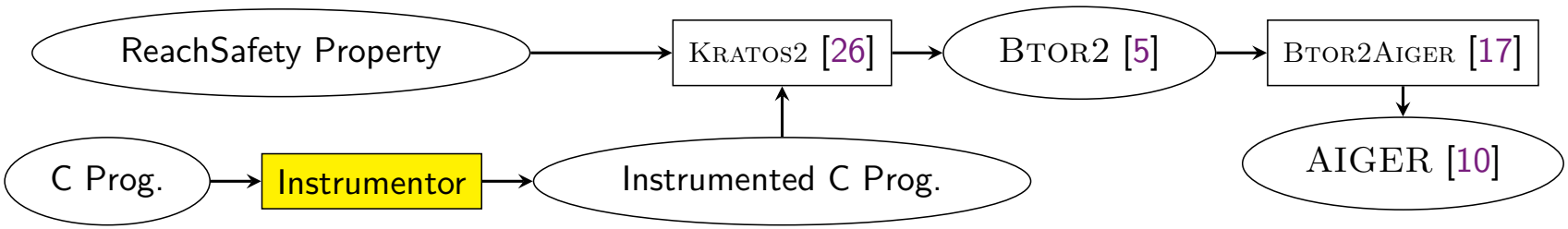
CPV ranks 6$^{\text{th}}$ out of 26 in *ReachSafety* as a first-time participant in SV-COMP 2024!

Software Architecture of CPV



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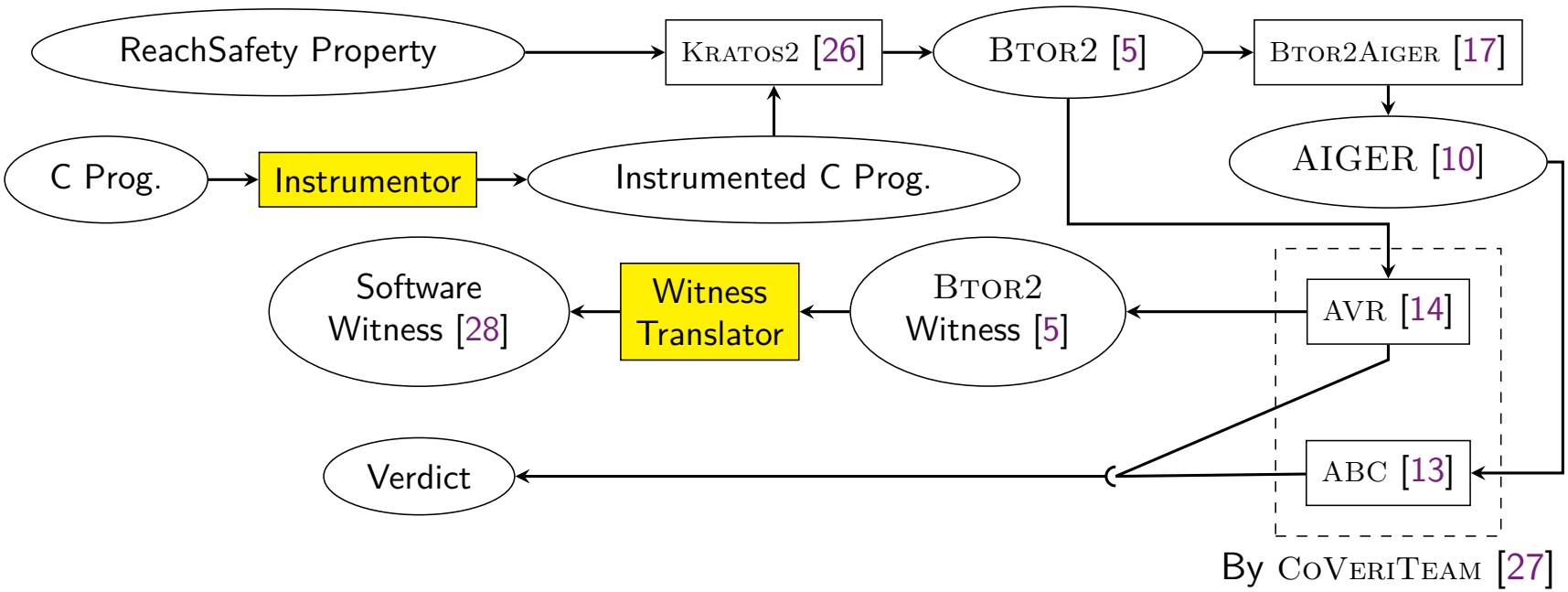

- Program instrumentation for retrieving witness information
- HW-to-SW witness translation

Agenda

1. Cross-application of HW and SW formal verification
1.1 Applying SW analyzers to HW verification tasks
1.2 Applying HW model checkers to SW verification tasks

2. Knowledge consolidation of formal verification
2.1 Transferability of HW algorithms to SW verification

3. Reflection and outlook

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A Transferability Study of Interpolation-Based Hardware Model Checking to Software Verification

Dirk Beyer, Po-Chun Chien, Marek Jankola, and Nian-Ze Lee

LMU Munich, Germany




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Characteristics of two interpolation-based algorithms [30, 31] for hardware are shown to be transferrable to software.

Transferring HV Studies to SV Contexts

- Implement two hardware-verification algorithms in CPAchecker and evaluate on ∼9 K software tasks
  - Baseline: *interpolation-based model checking* (IMC) [32] (software adoption to appear in *JAR* [4])

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- Interpolation-Sequence-Based Model Checking, 2009 [30]
  - Benchmark set: 136 tasks derived from industrial designs
  - Claims
    - Faster than IMC on unsafe tasks (✓)
    - Faster than IMC on safe tasks if higher unrolling (?)
    - Overall, faster than IMC (by 30 %) (?)

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- Interpolation-Sequence-Based Model Checking, 2009 [30]
- Intertwined Forward-Backward Reachability Analysis Using Interpolants, 2013 [31]
  - Benchmark set: 37 tasks derived from industrial designs
  - Claims
    - Local strengthening enough to refute spurious bugs (✓)
    - Faster than IMC on safe tasks (?)
    - Computes more interpolants than IMC (✓)
    - More sensitive to the sizes of interpolants (?)
    - Overall, faster than IMC (by 36 %) (?)

Summary

- Transferability of algorithmic characteristics confirmed
  - Interpolation-sequence faster to find bugs
  - Local strengthening enough to refute spurious bugs
- Unifying knowledge across hardware and software for full-stack system verification

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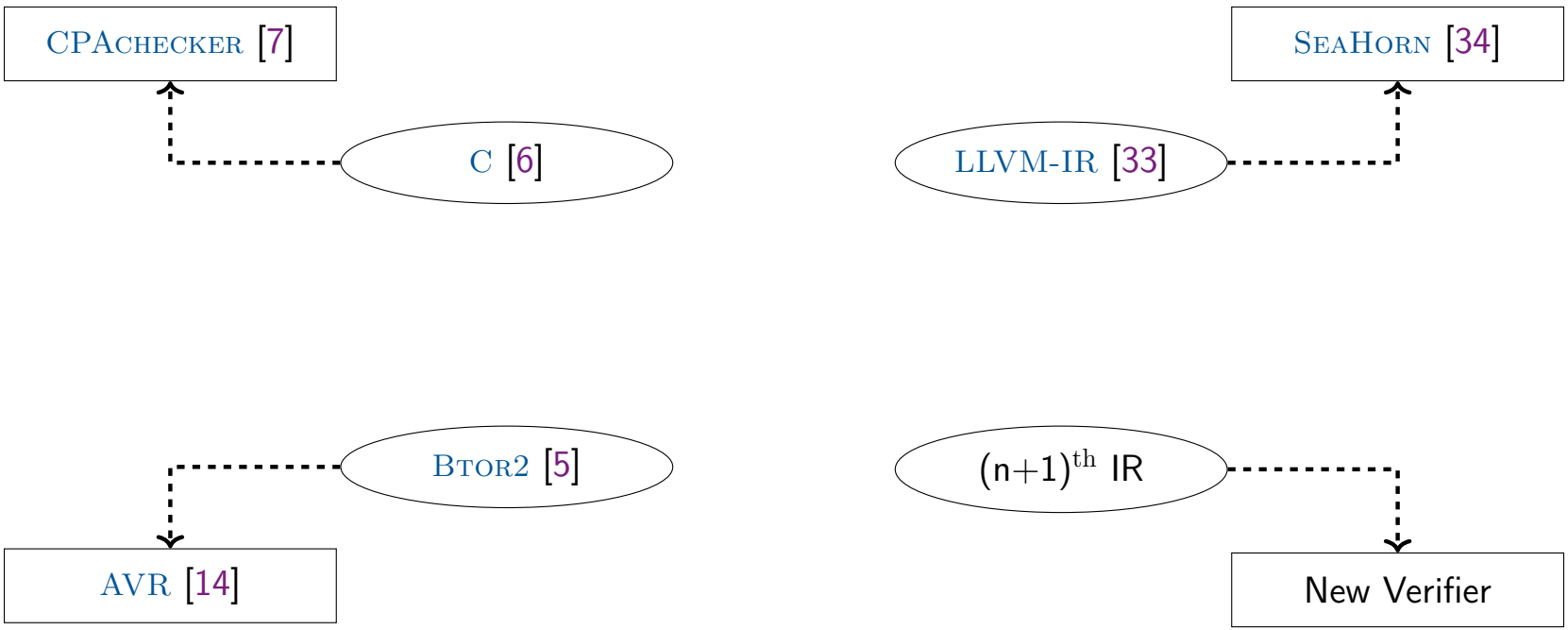
Bridging HW and SW Analysis: So Far

- SW tools uniquely solving HW tasks [1, 2]
- HV algorithms [4] and tools [3] improving SV
- Transferability of algorithmic characteristics [29]

Critical Reflection



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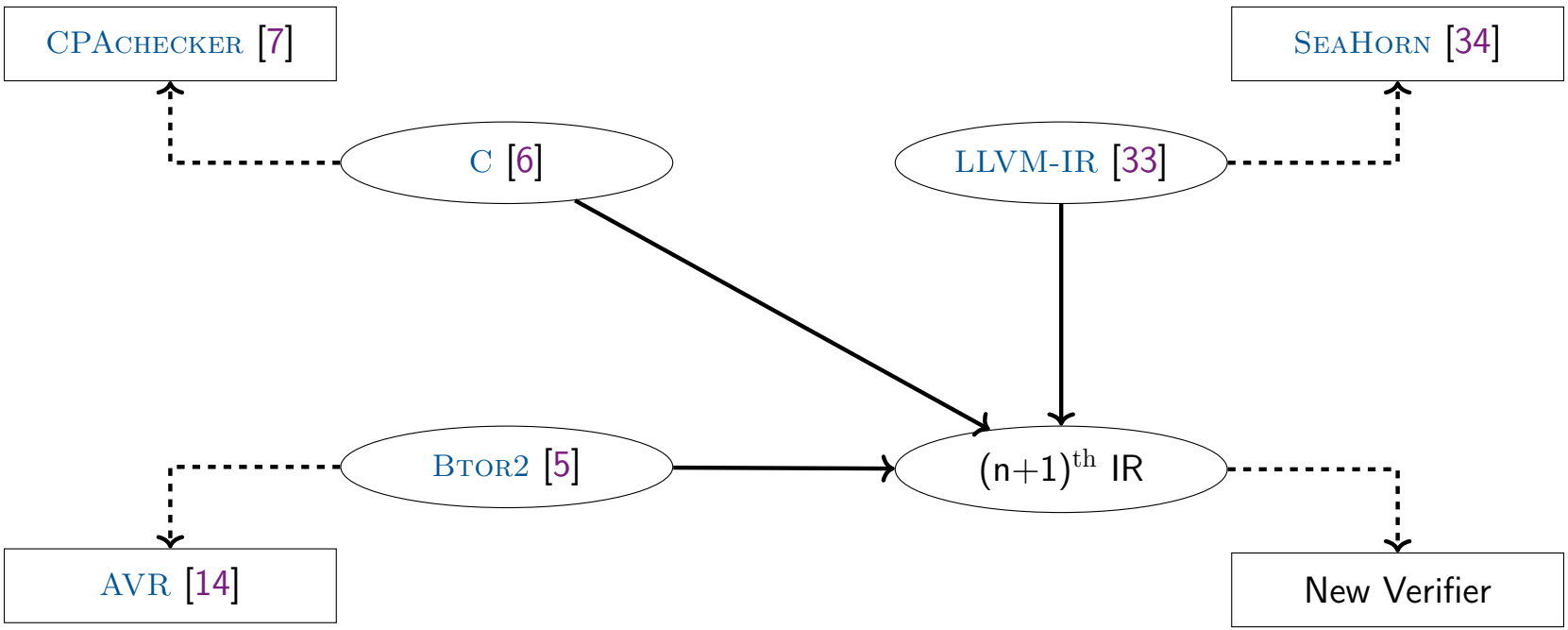

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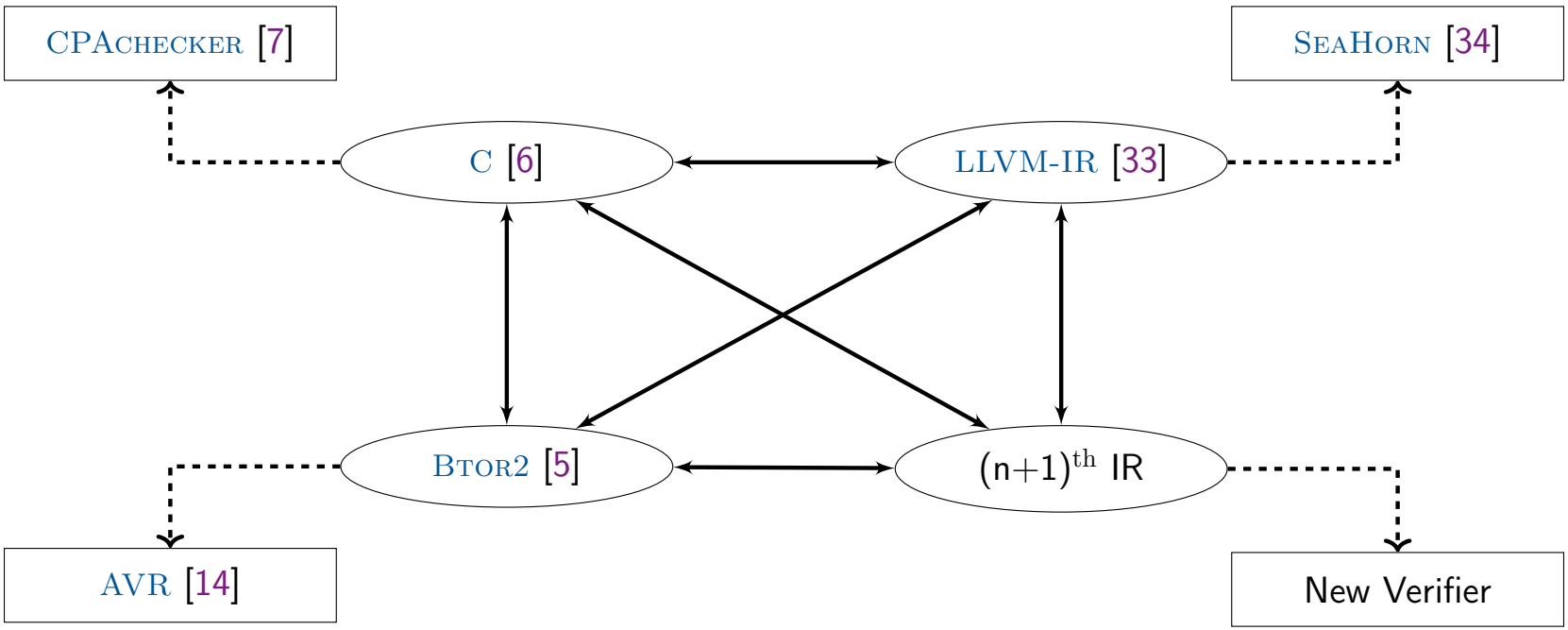

Transformation between different representations to leverage their unique strengths

Challenges of Heterogeneous Systems

- Firmware
  - Ex: data privacy of smart devices
  - Specific constructs (e.g., assembly), hardware modeling
  - Current practices: manual review or testing
  - Idea: circuit-based program verification

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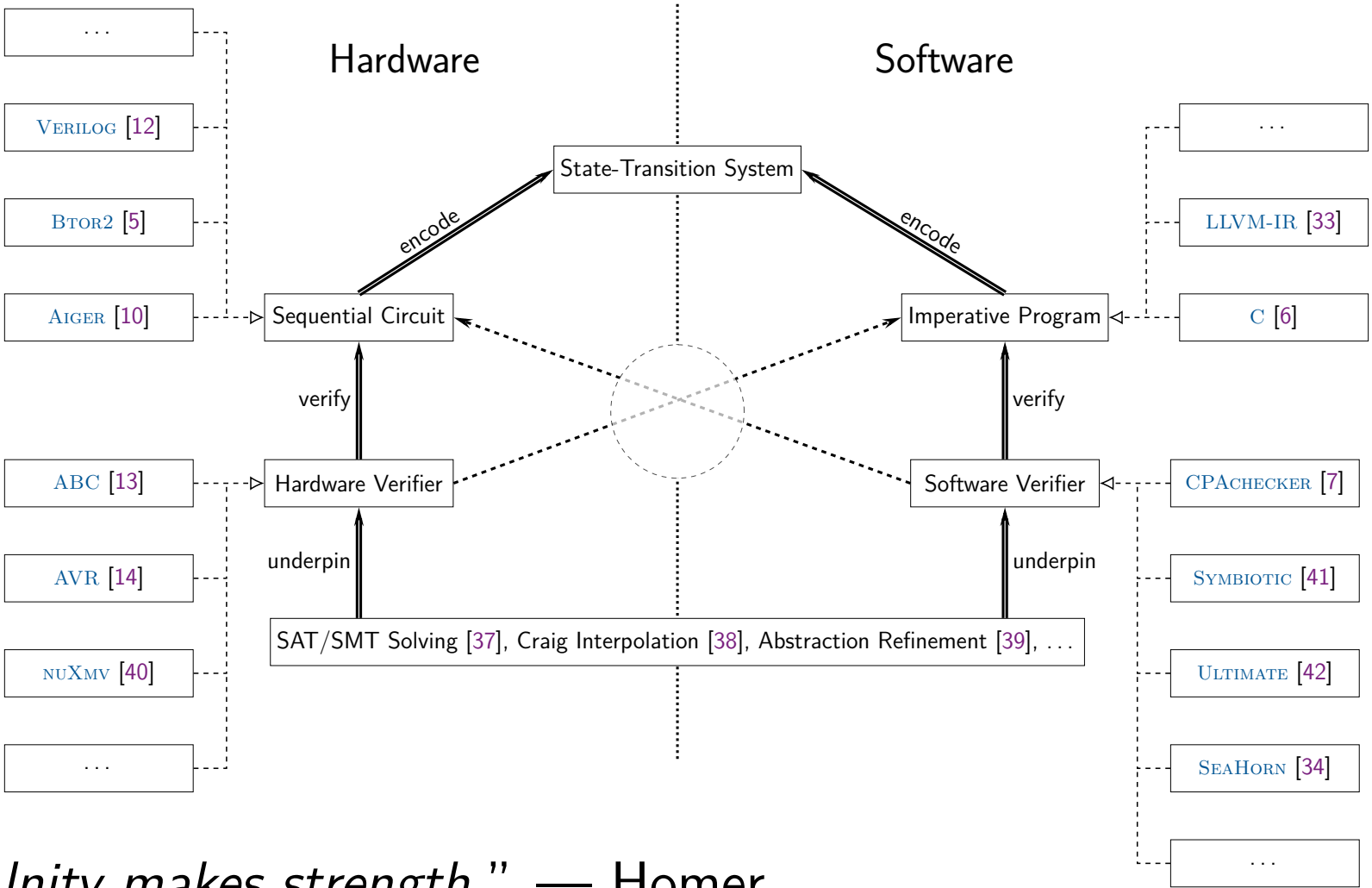
    - Less on C implementations (e.g., NeuroCodeBench [35])
  - Idea: symbolic computer algebra
- Hardware/software co-design (embedded systems)
  - Current practices: lower level verification conditions [36]
  - Idea: on-the-fly translation and abstraction as HW or SW

Closing the Gap between HW and SW Analysis



"*Unity makes strength.*" — Homer

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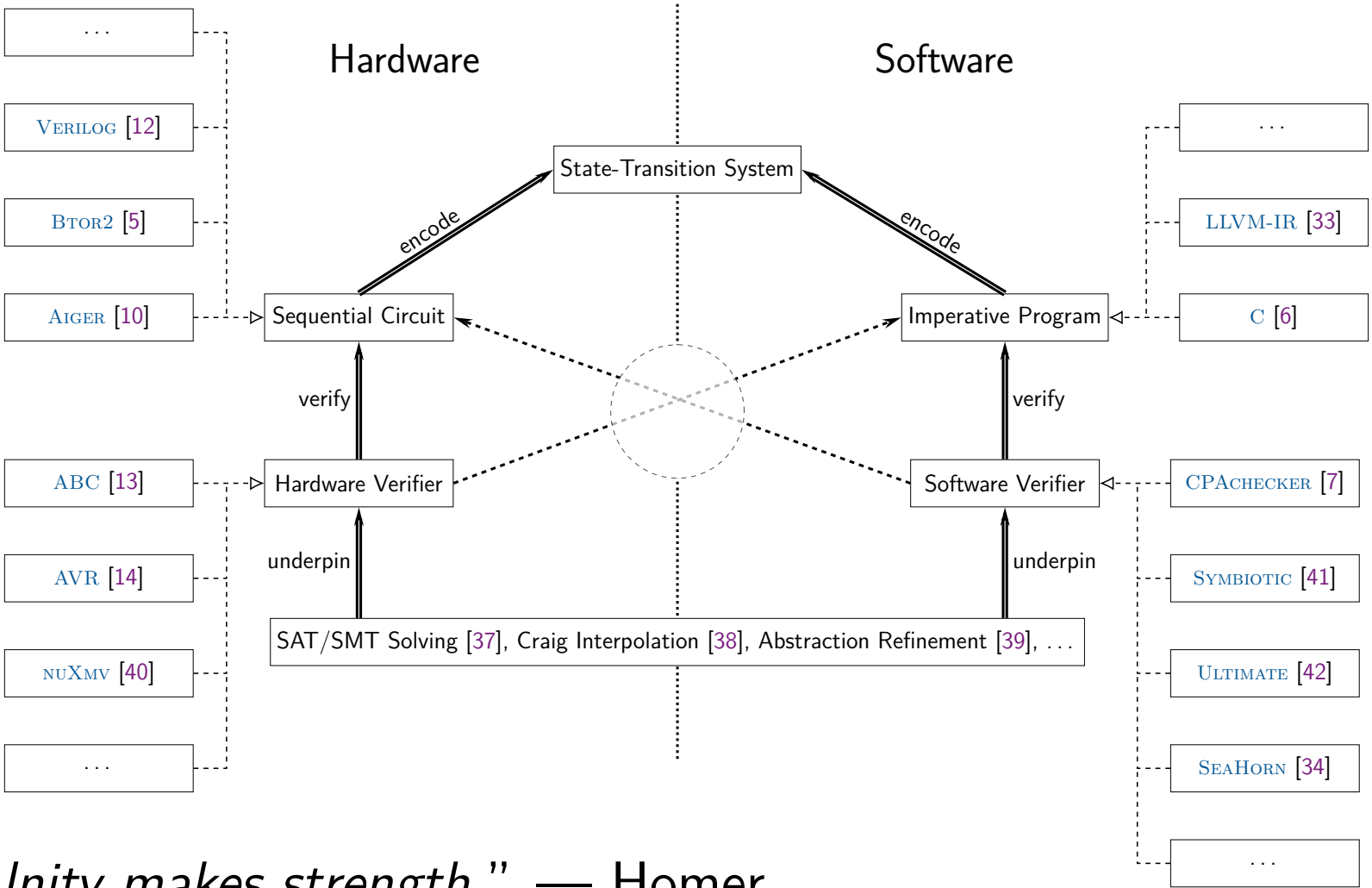

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We are hiring! (A full Ph.D. position funded by DFG)

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