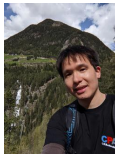


Exploring the Interplay of Hardware and Software Analysis

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2024-09-27 @ EDA Group Information Session



About Me

- ▶ 2014: B.Sc. in Electrical Engineering, NTU
- ▶ 2021: Ph.D. in Electronics Engineering, NTU
- ▶ 2021-2024: PostDoc in Computer Science, LMU Munich, Germany
- ▶ From 2025: Assistant Professor, EDA Group, NTU

About Me

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Research interests: formal methods and verification for computational models (hardware, software, and more)

Formal Verification in a Nutshell

- ▶ Does a **computational model** satisfy a **specification**?
 - ▶ Model: control-flow automata (software), sequential circuits (hardware), etc.
 - ▶ Specification: temporal-logic formulas

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 - ▶ Specification: temporal-logic formulas
 - ▶ Mathematical rigor: prove absence of bugs (cf. testing)
 - ▶ Undecidable in theory

Facebook's Software Verifier Infer [1]

```
class Infer {  
  
    String mayReturnNull(int i) {  
        if (i > 0) {  
            return "Hello, Infer!";  
        }  
        return null;  
    }  
  
    int mayCauseNPE() {  
        String s = mayReturnNull(0);  
        return s.length();  
    }  
  
}
```

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    int mayCauseNPE() {  
        String s = mayReturnNull(0);  
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    }  
  
}
```

```
Found 1 issue  
Infer.java:12: error: NULL_DEREFERENCE  
    object s last assigned on line 11 could be null and is dereferenced at line 12  
10.     int mayCauseNPE() {  
11.         String s = mayReturnNull(0);  
12. >     return s.length();  
13.     }
```

Overview of Software Verification

- ▶ Automatically detect issues in source code
 - ▶ Null-pointer dereference
 - ▶ Assertion violation
 - ▶ Memory leak
 - ▶ ...

Overview of Software Verification

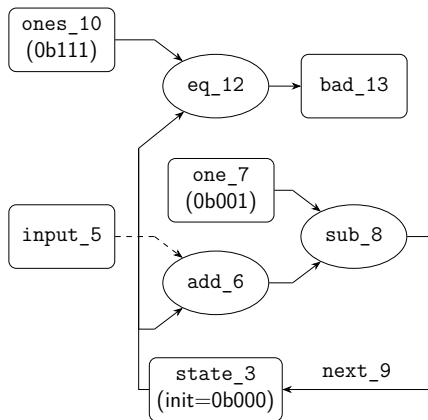
- ▶ Automatically detect issues in source code
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- ▶ Annual tool competitions: [SV-COMP](#)
 - ▶ 59 tools on more than 30 K verification tasks in 2024 [2]

Overview of Software Verification

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 - ▶ ...
- ▶ Annual tool competitions: [SV-COMP](#)
 - ▶ 59 tools on more than 30 K verification tasks in 2024 [2]
- ▶ CPACHECKER [3]: found more than 100 bugs (confirmed and fixed) in [Linux kernel modules](#) [4]

Example: Sequential Circuit in the BTOR2 Language

```
1 sort bitvec 3
2 zero 1
3 state 1
4 init 1 3 2
5 input 1
6 add 1 3 5
7 one 1
8 sub 1 6 7
9 next 1 3 8
10 ones 1
11 sort bitvec 1
12 eq 11 3 10
13 bad 12
```



Translating BTOR2 Circuits to C Programs

```
1 sort bitvec 3
2 zero 1
3 state 1
4 init 1 3 2
5 input 1
6 add 1 3 5
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8 sub 1 6 7
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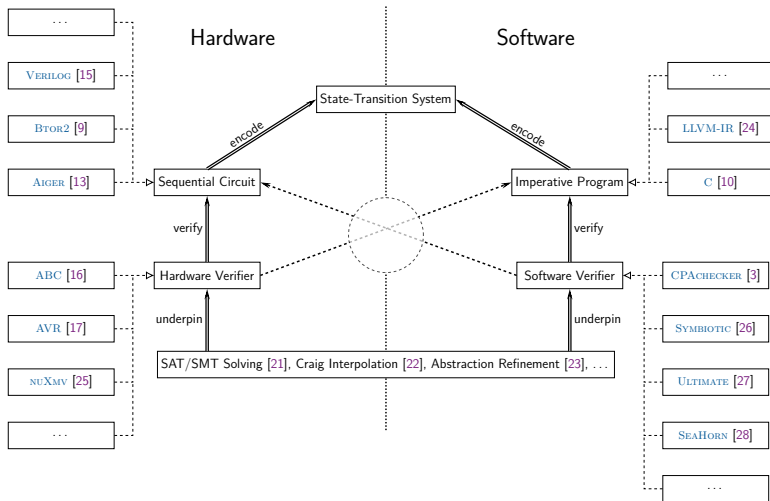
```
1 void main() {
2     typedef unsigned char SORT_1;
3     typedef unsigned char SORT_11;
4     const SORT_1 var_2 = 0b000;
5     const SORT_1 var_7 = 0b001;
6     const SORT_1 var_10 = 0b111;
7     SORT_1 state_3 = var_2;
8     for (;;) {
9         SORT_1 input_5 = nondet_uchar();
10        input_5 = input_5 & 0b111;
11        SORT_11 var_12 = state_3 == var_10;
12        SORT_11 bad_13 = var_12;
13        if (bad_13) { ERROR: abort(); }
14        SORT_1 var_6 = state_3 + input_5;
15        var_6 = var_6 & 0b111;
16        SORT_1 var_8 = var_6 - var_7;
17        var_8 = var_8 & 0b111;
18        state_3 = var_8;
19    }
20 }
```

Circuit-Based Program Verification

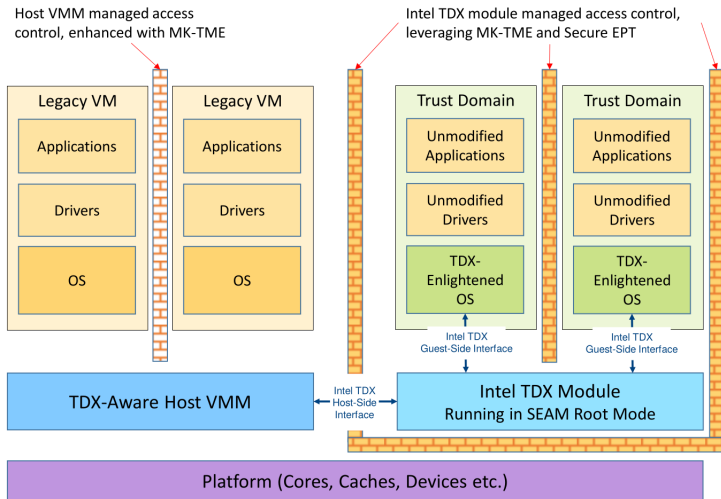
- ▶ **Sequential circuit** as an intermediate representation for program analysis
 - ▶ Leveraging hardware verification and logic synthesis

Our circuit-based program verifier, CPV, ranks 6th out of 26 in the category *ReachSafety* as a first-time participant in SV-COMP 2024!

Exploring the Interplay of Hardware and Software Verification

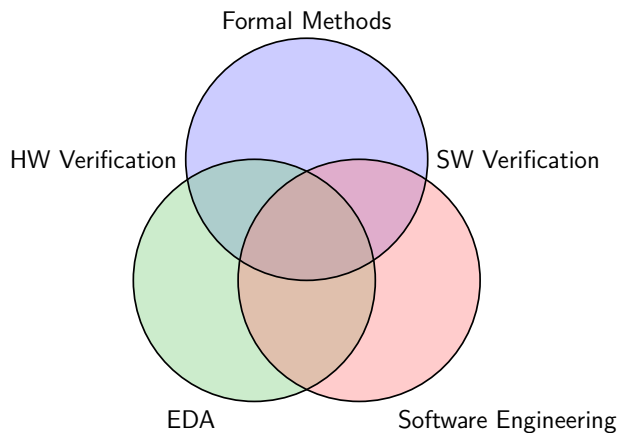


Emerging Paradigms: Confidential Computing in the Cloud



Source: Figure 2.1 in [Intel TDX Module v1.5 Base Architecture Specification](#)

We Are Looking for You!



- ▶ International collaboration
- ▶ Industrial collaboration



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