Formal **M**ethods and **A**nalysis for **C**omputing and **E**ngineering

Prof. Nian-Ze Lee
nzlee@ntu.edu.tw

ForMACE Lab, National Taiwan University

February 24, EDA Seminar 2025

Agenda

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Who Am I?

- A new faculty member at NTUEE/GIEE (starting from February)
- A PostDoc at LMU Munich, Germany, from 2021 to 2024
- A PhD graduate from GIEE in 2021
- A Bachelor's graduate from NTUEE in 2014

What Do I Research and Teach?

- Formal Methods

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- Formal Methods

A new course this semester: every Tuesday from 14:20 to 17:30 in EE2-225

Agenda

Problems with This Code

```
1       int binarySearch(int arr[], int left, int right, int target) {
2         while (left <= right) {
3             int mid = (left + right) / 2;
4             if (arr[mid] = target)
5                 return mid;
6             if (arr[mid] < target)
7                 left = mid;
8             else
9                 right = mid;
10        }
11      }
```

How would you debug the code?

Problems with This Code

```
1   int binarySearch(int arr[], int left, int right, int target) {
2     while (left <= right) {
3         // Bug 1: Potential integer overflow when computing mid
4         // Found in "java.util.Arrays" in 2006
5         int mid = (left + right) / 2;
6         // Bug 2: Incorrect comparison (assignment instead of comparison)
7         if (arr[mid] = target)
8             return mid;
9         // Bug 3: Incorrect updates to left and right may cause infinite loop
10        if (arr[mid] < target)
11            left = mid;
12        else
13            right = mid;
14    }
15    // Bug 4: Forgetting to return a value may cause undefined behavior
16  }
```

Problems with This Code

```
1   int binarySearch(int arr[], int left, int right, int target) {
2     while (left <= right) {
3         // Fix 1: Prevent overflow
4         int mid = left + (right - left) / 2;
5         // Fix 2: Use comparison
6         if (arr[mid] == target)
7             return mid;
8         // Fix 3: Update left and right correctly
9         if (arr[mid] < target)
10            left = mid + 1;
11        else
12            right = mid - 1;
13    }
14    // Fix 4: Return -1 to indicate target not found
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```

Q: Can we exhaustively debug the code without running test cases?
A: Formal Methods!

Demo: CPAchecker

- Automatic and static program analyzer for C programs
- Found more than 100 bugs (confirmed and fixed) in Linux kernel modules
- Top contender at annual competitions for software verifiers (SV-COMP)

“Formal” Methods in a Nutshell

- Modeling computing systems and specifying their expected behaviors so that we can (automatically) analyze their correctness with mathematical rigor
  - Automata, logic, constraint solving, etc.

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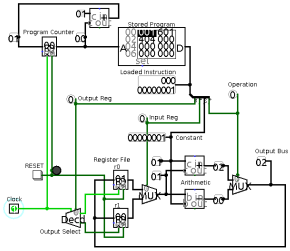
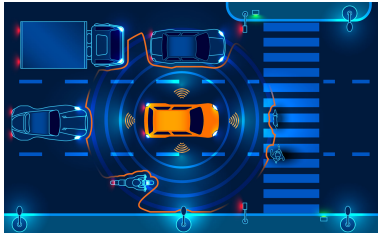
- What does "formal" mean?
  - "Form" is the key: $(A \Rightarrow B) \wedge (B \Rightarrow C) \Rightarrow (A \Rightarrow C)$
- Comparison with testing
  - Static vs. Dynamic
  - Symbolic vs. Concrete
  - All possibilities (hard!) vs. Some test cases

Agenda

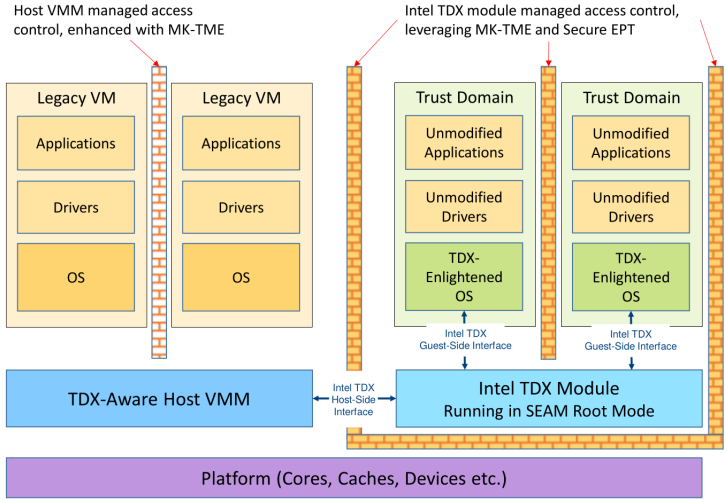
Engineering of Software, Hardware, and Cyber-Physical Systems





*Images from the Internet

Case Study: Confidential Computing for Data Security in Cloud



Source: Figure 2.1 in Intel TDX Module v1.5 Base Architecture Specification

Agenda

Btor2-Cert: A Certifying Hardware-Verification Framework Using Software Analyzers

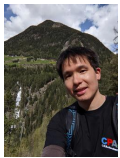
Zsófia Ádám[1,2], Dirk Beyer[2], Po-Chun Chien[2], Nian-Ze Lee[2], and Nils Sirrenberg[2]

[1]Budapest University of Technology and Economics, Hungary

[2]LMU Munich, Germany

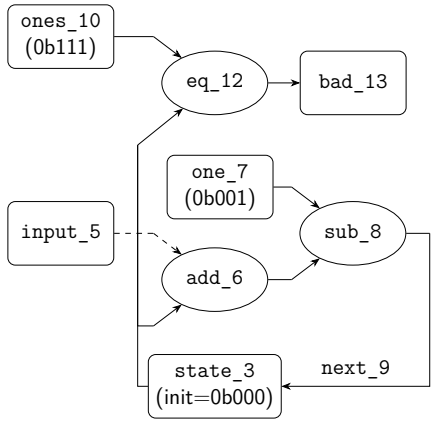
Received "Distinguished Artifact Award" at TACAS 2024




The BTOR2 Language

```
1 sort bitvec 3
2 zero 1
3 state 1
4 init 1 3 2
5 input 1
6 add 1 3 5
7 one 1
8 sub 1 6 7
9 next 1 3 8
10 ones 1
11 sort bitvec 1
12 eq 11 3 10
13 bad 12
```



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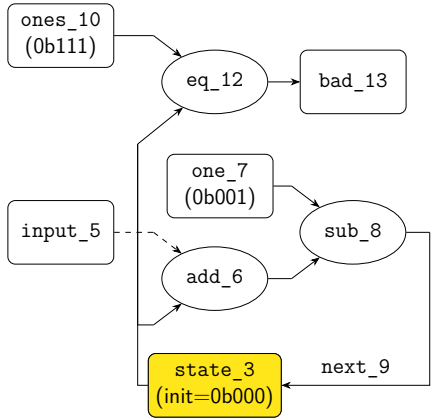

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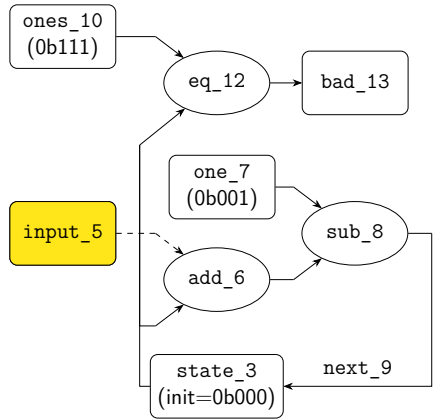

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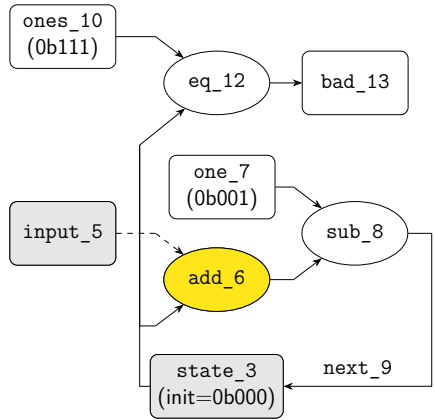

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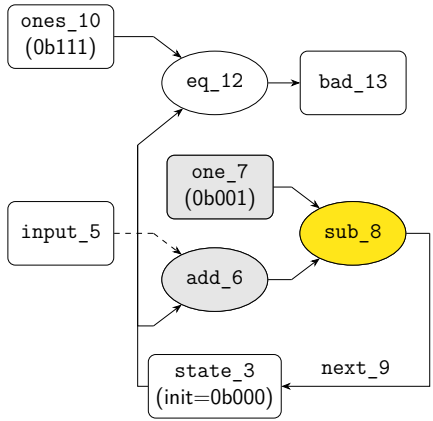

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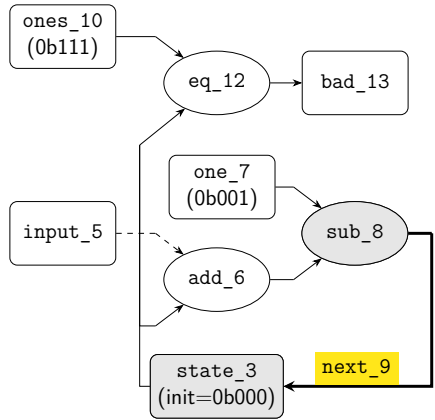

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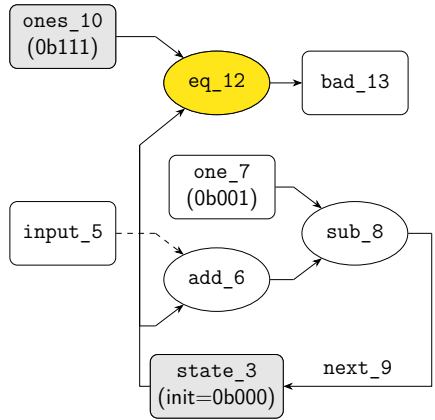

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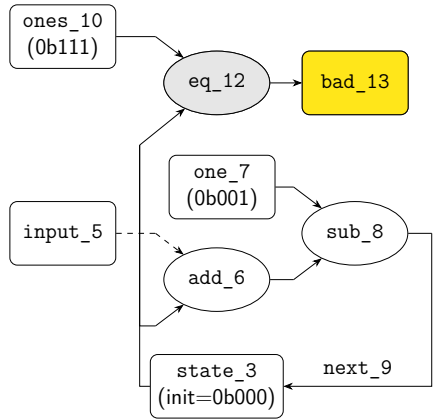

Translating BTOR2 Circuits to C Programs

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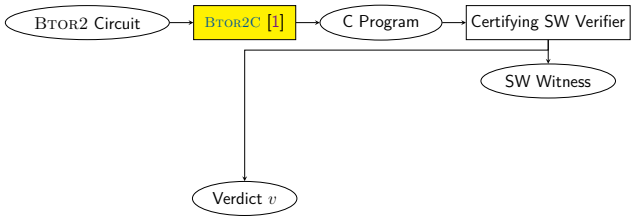
```

```c
void main() {
  typedef unsigned char SORT_1;
  typedef unsigned char SORT_11;
  const SORT_1 var_2 = 0b000;
  const SORT_1 var_7 = 0b001;
  const SORT_1 var_10 = 0b111;
  SORT_1 state_3 = var_2;
  for (;;) {
    SORT_1 input_5 = nondet_uchar();
    input_5 = input_5 & 0b111;
    SORT_11 var_12 = state_3 == var_10;
    SORT_11 bad_13 = var_12;
    if (bad_13) { ERROR: abort(); }
    SORT_1 var_6 = state_3 + input_5;
    var_6 = var_6 & 0b111;
    SORT_1 var_8 = var_6 - var_7;
    var_8 = var_8 & 0b111;
    state_3 = var_8;
  }
}
```

Certifying Verification for BTOR2 with SV Tools



- BTOR2 [5] word-level circuits and translator BTOR2C [1]
- Software verifiers in SV-COMP [18]

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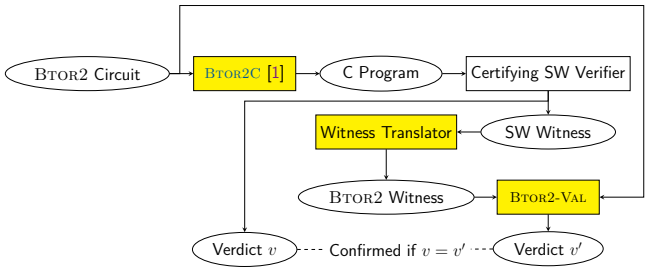

- BTOR2 [5] word-level circuits and translator BTOR2C [1]
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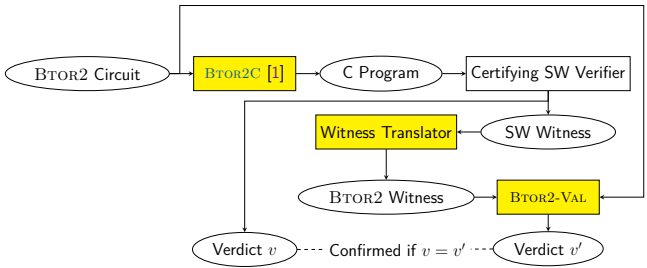
- Software-to-hardware witness translation and BTOR2-VAL

Certifying Verification for BTOR2 with SV Tools



- BTOR2 [5] word-level circuits and translator BTOR2C [1]
- Software verifiers in SV-COMP [18]
- Software-to-hardware witness translation and BTOR2-VAL
- On 1214 BTOR2 circuits, BTOR2-CERT
  - found 37 bugs that ABC [13] missed using CBMC [19]
  - derived invariants to accelerate ABC using CPACHECKER [7]

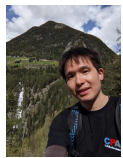
Summary

- Btor2-Cert: certifying and validating hardware verifier using software verifiers
- Reproduction artifact [20] available on Zenodo
  - **Distinguished Artifact Award** at TACAS 2024

CPV: A Circuit-Based Program Verifier

Po-Chun Chien and Nian-Ze Lee

LMU Munich, Germany



Research Question

- Sequential circuit as an intermediate representation for program analysis
  - Leveraging hardware model checkers as backend

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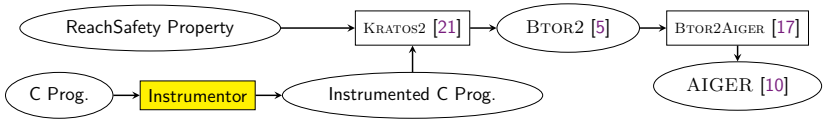
CPV ranked 6th out of 26 in the category *ReachSafety* as a first-time participant in SV-COMP 2024. (and a higher position in 2025!)

Software Architecture of CPV



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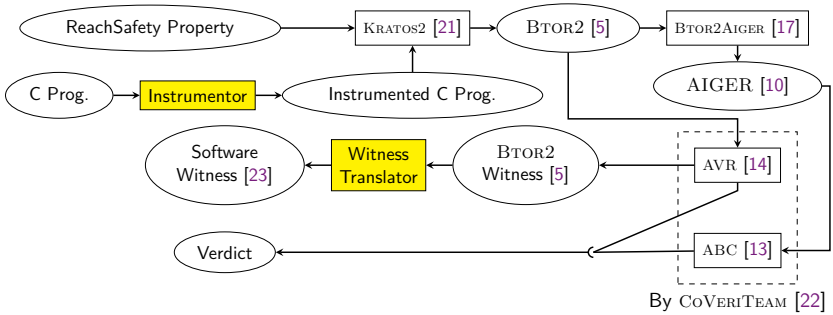

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- Software-to-hardware translation by Kratos2 [21]
- Translated circuits verified by hardware model checkers
- Hardware-to-software witness translation

Agenda

Confidential Computing

- Scenario: sensitive data to train ML models using cloud services

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  $\rightarrow$ Do not want to trust cloud operators

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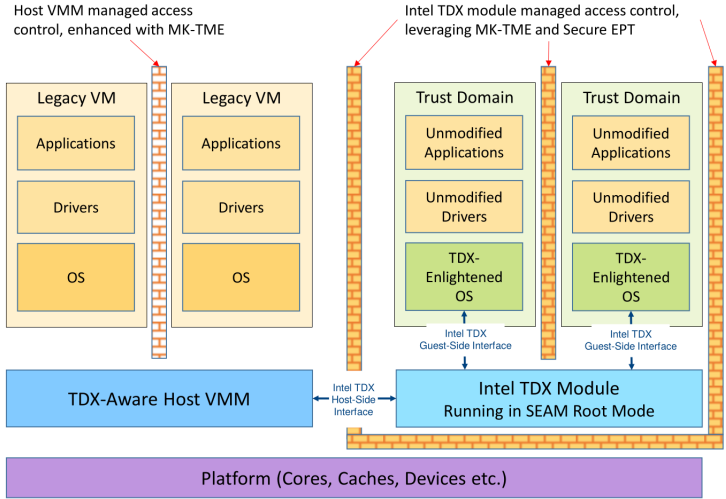
How can we protect data when they are in use, especially in a remote execution environment, e.g., cloud?

Intel Trust Domain Extensions (TDX)



Source: Figure 2.1 in Intel TDX Module v1.5 Base Architecture Specification

Intel TDX: Components

- Hardware extensions: new CPU mode, highest privilege
- Firmware components: TDX module
  - Loaded in special memory range
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Goal: verify ABIs of TDX module (implemented as C code plus assembly), assuming VMM and TDs can call any ABI with any inputs

Intel TDX: Specification for ABI Function `TDG.SYS.RD`

Table 5.324: TDG.SYS.RD Input Operands Definition

Operand	Description		
RAX	TDCALL instruction leaf number and version, see 5.4.1		
	Bits	**Field**	**Description**
	15:0	Leaf Number	Selects the TDCALL interface function
	23:16	Version Number	Selects the TDCALL interface function version Must be 0
	63:24	Reserved	Must be 0
RDX	Field identifier – see 3.10 The LAST_ELEMENT_IN_FIELD and LAST_FIELD_IN_SEQUENCE components of the field identifier must be 0. WRITE_MASK_VALID, INC_SIZE, CONTEXT_CODE and ELEMENT_SIZE_CODE components of the field identifier are ignored. A value of -1 is a special case: it is not a valid field identifier; in this case the first readable field identifier is returned in RDX.		

Table 5.325: TDG.SYS.RD Output Operands Definition

Operand	Description
RAX	TDCALL instruction return code – see 5.4.1
RDX	If the input field identifier was -1, RDX returns the first readable field identifier. Else, in case of an error, RDX returns -1. On success, RDX returns the next readable field identifier. A value of -1 indicates no next field identifier is available.
R8	Contents of the field In case of no success, as indicated by RAX, R8 returns 0.
Other	Unmodified

Source: Intel TDX Module v1.5 ABI Specification

Firmware-Specific Constructs

- Byte/Bit-precise modeling of memory layouts (type punning)
- Inline assembly
- Externally defined variables

Example of Inline Assembly: Access Loader-Defined Variables

```
1  _STATIC_INLINE_ tdx_module_local_t* get_local_data(void) {
2    uint64_t local_data_addr;
3    _ASM_("movq %%gs:%c[local_data], %0\n\t"
4          : "=r"(local_data_addr)
5          : [local_data] "i"(
6              offsetof(tdx_module_local_t, local_data_fast_ref_ptr)));
7    return (tdx_module_local_t*)local_data_addr;
8  }
```

Modeling Inline Assembly via Program Instrumentation

```
1  _STATIC_INLINE_ tdx_module_local_t* get_local_data(void) {
2  #ifdef TDXFV_NO_ASM
3    return &local_data_fv;
4  #else
5    uint64_t local_data_addr;
6    _ASM_("movq %%gs:%c[local_data], %0\n\t"
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10   return (tdx_module_local_t*)local_data_addr;
11 #endif
12 }
```
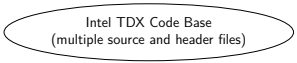
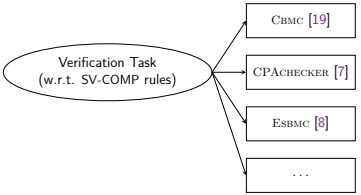

HarnessForge: Generating Verification Tasks Intel TDX





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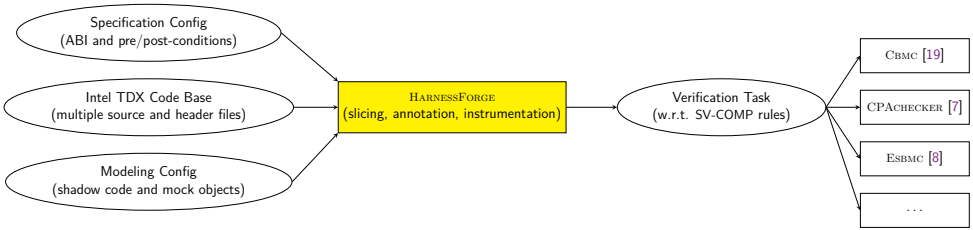

- Slice off irrelevant code
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- Instrument shadow C code to model inline assembly

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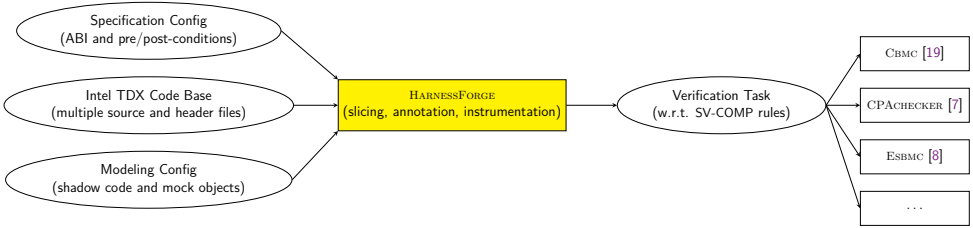

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Vision: extend HarnessForge to arbitrary code base
(integrated into the build process, like common testing frameworks)

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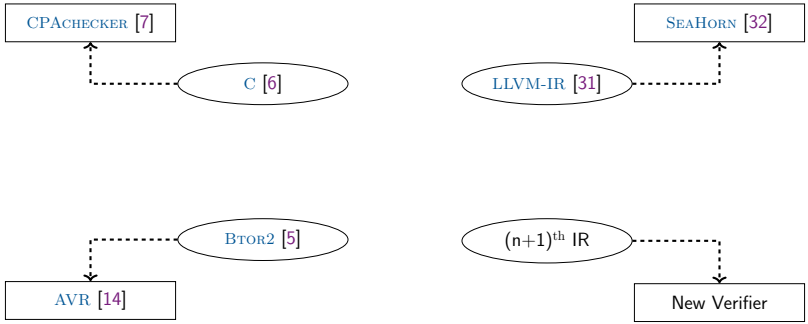
Intersection of Hardware and Software Verification: So Far

- Software analyzers uniquely solving hardware tasks [1, 2]
- Hardware-verification algorithms [4] and tools [3] improving software analysis
- Transferability of algorithmic characteristics [24]
- Firmware verification requiring expertise of both sides

Critical Reflection: The Transformation Game [30]



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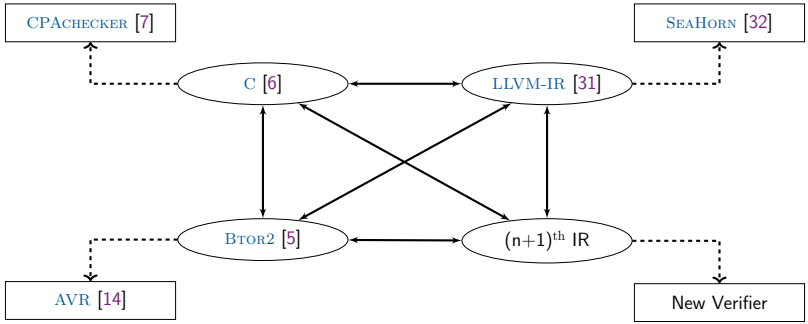

Developing a transformation network between different representations to leverage their unique strengths

Practical Verification Challenges

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  - Ex: used in confidential computing to protect data security in the cloud
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  - Gap: mathematical operations (e.g., sigmoid function)
- Hardware/software co-design (embedded systems)
  - Ex: hardware accelerators
  - Current practices: lower level verification conditions [34]
  - Gap: scalability and lack of modularity

Welcome to ForMACE Lab!

- Multiple positions at NTU and LMU Munich
- Working at the intersection of
  - Hardware vs. Software (and more!)
  - Academic tools vs. Industrial applications
- New course "Formal Methods" (EE2-225, every Tuesday)
- Contact: nzlee@ntu.edu.tw (Office: EE2-349)

https://formace-lab.gitlab.io/webpage/

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